What is claimed is:

1. An arithmetic device able to reconfigure an operation path by outside control, comprising

a first selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a second selecting means for selecting desired data from a plurality of input data in accordance with a control signal, and

an arithmetic means receiving as input the output signal of the first selecting means and the output signal of the second selecting means and performing operations in accordance with instructions of a control signal.

2. An arithmetic device as set forth in claim 1, wherein the arithmetic means performs dyadic operation.

3. An arithmetic device as set forth in claim 2, wherein the arithmetic means performs monadic operation on the result of the dyadic operation.

4. An arithmetic device as set forth in claim 1, further comprising a delay means for outputting the input data delayed by an amount of delay according to a control signal.

5. An arithmetic device able to reconfigure an

operation path by outside control, comprising:

a first selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a second selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a third selecting means for selecting desired data from a plurality of input data in accordance with a control signal, and

an arithmetic means receiving as input the output signal of the first selecting means, the output signal of the second selecting means, and the output signal of the third selecting means and performing operation in accordance with instructions of a control signal.

6. An arithmetic device as set forth in claim 5, wherein the arithmetic means performs trinomial operation.

7. An arithmetic device as set forth in claim 6, wherein the arithmetic means performs monadic operation on the result of the trinomial operation.

8. An arithmetic device as set forth in claim 5, further comprising a delay means for outputting the input data delayed by an amount of delay according to a control

signal.

9. An arithmetic device able to reconfigure an operation path by outside control, comprising:

a first selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a second selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a third selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a first arithmetic means receiving as input the output signal of the first selecting means and the output signal of the second selecting means and performing operation in accordance with instructions of a control signal, and

a second arithmetic means receiving as input the output signal of the first selecting means and the output signal of the second selecting means and third selecting means and performing operation in accordance with instructions of a control signal.

10. An arithmetic device as set forth in claim 9, further comprising a fourth selecting means for selecting one of the output signal of the first arithmetic means

and the output signal of the second arithmetic means in accordance with a control signal.

11. An arithmetic device as set forth in claim 9, wherein the first arithmetic means performs dyadic operation, while the second arithmetic means performs trinomial operation.

12. An arithmetic device as set forth in claim 11, wherein the first arithmetic means performs monadic operation on the result of the dyadic operation, while the second arithmetic means performs monadic operation on the result of the trinomial operation.

13. An arithmetic device as set forth in claim 9, further comprising a delay means for outputting the input data delayed by an amount of delay according to a control signal.

14. An arithmetic device able to reconfigure an operation path by outside control, comprising:

a first selecting means for selecting one data from a first data group in accordance with a control signal,

a second selecting means for selecting one data from a second data group in accordance with a control signal,

a first arithmetic means for receiving as input the output signal of the first selecting means and the

output signal of the second selecting means and performing operation in accordance with instructions of a control signal,

a second arithmetic means for receiving as input the output signal of the first selecting means and the output signal of the second selecting means and performing operation in accordance with instructions of a control signal, and

a third selecting means for selecting one of the output signal of the first arithmetic means and the output signal of the second arithmetic means.

15. An arithmetic device able to reconfigure an operation path by outside control, comprising:

a first selecting means for selecting one data from a first data group in accordance with a control signal,

a second selecting means for selecting one data from a second data group in accordance with a control signal,

a third selecting means for selecting one data of a third data group in accordance with a control signal,

a first arithmetic means for receiving as input at least two signals among the output signal of the first selecting means, the output signal of the second

selecting means, and the output signal of the third selecting means and performing operation in accordance with instructions of a control signal,

a second arithmetic means for receiving as input at least two signals among the output signal of the first selecting means, the output signal of the second selecting means, and the output signal of the third selecting means and performing operation in accordance with instructions of a control signal, and

a fourth selecting means for selecting one of the output signal of the first arithmetic means and the output signal of the second arithmetic means.

16. A parallel arithmetic device having a plurality of arithmetic devices, each comprising:

a first selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a second selecting means for selecting desired data from a plurality of input data in accordance with a control signal, and

an arithmetic means receiving as input the output signal of the first selecting means and the output signal of the second selecting means in accordance with a control signal and

able to reconfigure an operation path by

outside control,

connects the inputs and outputs of data of the plurality of arithmetic devices in cascade, and

supplies the operation result signal of an arithmetic device as one data of a plurality of data inputs of another device.

17. A parallel arithmetic device as set forth in claim 16, further comprising a delay means for delaying the input data by an amount of delay in accordance with a control signal and outputting it to the arithmetic device of the next stage.

18. A parallel arithmetic device having a plurality of arithmetic devices, each comprising:

a first selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a second selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a third selecting means for selecting desired data from a plurality of input data in accordance with a control signal, and

an arithmetic means receiving as input the output signal of the first selecting means, the output signal of the second selecting means, and the output

signal of the third selecting means and performing operation in accordance with instructions of a control signal and

able to reconfigure an operation path under outside control,

connects in cascade the inputs and outputs of data of the plurality of arithmetic devices, and

supplies the operation result signal of an arithmetic device as one data of the plurality of data inputs of another device.

19. A parallel arithmetic device as set forth in claim 18, further comprising a delay means for delaying the input data by an amount of delay in accordance with a control signal and outputting it to the arithmetic device of the next stage.

20. A parallel arithmetic device having a plurality of arithmetic devices, each comprising:

a first selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a second selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a third selecting means for selecting desired data from a plurality of input data in accordance with a

control signal,

a first arithmetic means receiving as input the output signal of the first selecting means and the output signal of the second selecting means and performing operation in accordance with instructions of a control signal,

a second arithmetic means receiving as input the output signal of the first selecting means, the output signal of the second selecting means, and the output signal of the third selecting means and performing operation in accordance with instructions of a control signal, and

a fourth selecting means for selecting one of the output of the first arithmetic means and the output of the second arithmetic means in accordance with a control signal and outputting the same as an operation result signal and

able to reconfigure an operation path under outside control,

connects in cascade the inputs and outputs of data of the plurality of arithmetic devices, and

supplies the operation result signal of an arithmetic device as one data of the plurality of data inputs of another device.

21. A parallel arithmetic device as set forth

in claim 20, further comprising a delay means for delaying the input data by an amount of delay in accordance with a control signal and outputting it to the arithmetic device of the next stage.

22. A parallel arithmetic device having a plurality of arithmetic devices, each comprising:

a first selecting means for selecting one data from a first data group in accordance with a control signal,

a second selecting means for selecting one data from a second data group in accordance with a control signal,

a first arithmetic means receiving as input the output signal of the first selecting means and the output signal of the second selecting means and performing operation in accordance with instructions of a control signal,

a second arithmetic means receiving as input the output signal of the first selecting means and the output signal of the second selecting means and performing operation in accordance with instructions of a control signal, and

a third selecting means for selecting one of the output of the first arithmetic means and the output of the second arithmetic means in accordance with a

control signal and outputting the same as an operation result signal and

able to reconfigure an operation path under outside control,

connects in cascade the inputs and outputs of data of the first data group of the above plurality of arithmetic devices, and

supplies the operation result signal of an arithmetic device as one data of a second data group of another device.

23. A parallel arithmetic device as set forth in claim 22, further comprising a delay means for delaying the first data group by an amount of delay in accordance with a control signal and outputting it to the arithmetic device of the next stage.

24. A parallel arithmetic device having a plurality of arithmetic devices, each comprising:

a first selecting means for selecting one data from a first data group in accordance with a control signal,

a second selecting means for selecting one data from a second data group in accordance with a control signal,

a third selecting means for selecting one data from a third data group in accordance with a control

signal,

a first arithmetic means receiving as input at least two signals of the output signal of the first selecting means, the output signal of the second selecting means, and the output signal of the third selecting means and performing operation in accordance with instructions of a control signal,

a second arithmetic means receiving as input at least two signals of the output signal of the first selecting means, the output signal of the second selecting means, and the output signal of the third selecting means and performing operation in accordance with instructions of a control signal, and

a fourth selecting means for selecting one of the output of the first arithmetic means and the output of the second arithmetic means in accordance with a control signal and

able to reconfigure an operation path under outside control,

connects in cascade the inputs and outputs of data of the first data group and the second data group of the plurality of arithmetic devices, and

supplies the operation result signal of an arithmetic device as one data of a third data group of another device.

25. A parallel arithmetic device as set forth in claim 24 further comprising:

a first delay means for outputting the first data group to the arithmetic device of the next stage delayed by an amount of delay in accordance with a control signal and

a second delay means for outputting the second data group to the arithmetic device of the next stage delayed by exactly an amount of delay in accordance with a control signal.

26. An arithmetic device reconfigurable by outside control, comprising:

at least one computing unit having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal and outputting the operation results and

a plurality of input selection devices for selecting one data from the plurality of input data in accordance with a control signal and supplying the same to different inputs of the computing unit.

27. An arithmetic device as set forth in claim 26, further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data in the plurality of input data and supplying the operation

results to one input of the input selection device.

28. An arithmetic device reconfigurable by outside control, comprising:

at least one multiple input, multiple output computing unit each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs and

a plurality of output selection devices for selecting and outputting one data from the plurality of input data and the output data of the computing unit in accordance with a control signal.

29. An arithmetic device as set forth in claim 28, further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data in the plurality of input data and supplying the operation results to the output selection device.

30. An arithmetic device reconfigurable by outside control, comprising:

at least one computing unit having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal,

and outputting the operation results from the plurality of outputs,

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the computing unit, and

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and the output data of the computing unit in accordance with a control signal.

31. An arithmetic device as set forth in claim 30, further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data among the plurality of input data and supplying operation results to one input of the input selection devices and the output selection device.

32. An arithmetic device reconfigurable by outside control, comprising:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of input selection devices each

selecting one data from a plurality of input data in accordance with a control signal and supplying the same to different inputs of the first computing units, and

at least one second computing unit having a plurality of inputs and a plurality of outputs, supplied at the plurality of inputs with output data of the plurality of first computing units, performing a plurality of operations based on the plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of outputs.

33. An arithmetic device as set forth in claim 32, further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data in the plurality of input data and supplying the operation results to one input of the input selection device.

34. An arithmetic device reconfigurable by outside control, comprising:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

at least one second computing unit having a

plurality of inputs and a plurality of outputs, supplied at the plurality of inputs with output data of the plurality of first computing units, performing a plurality of operations based on the plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of outputs, and

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and the output data of at least one of the first and second computing units.

35. An arithmetic device as set forth in claim 34, wherein the plurality of output selection devices include:

a plurality of first output selection devices for selecting and outputting one data from a plurality of input data and output data of the first computing unit in accordance with a control signal and

a plurality of second output selection devices selecting and outputting one data from a plurality of input data, the output data of the first computing unit, and the output data of the second computing unit in accordance with a control signal.

36. An arithmetic device as set forth in claim 34, further comprising at least one monadic arithmetic means

for performing monadic operation on predetermined data in the plurality of input data and supplying the operation results to the output selection device.

37. An arithmetic device as set forth in claim 35, further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data in the plurality of input data and supplying the operation results to the first output selection device.

38. An arithmetic device reconfigurable by outside control, comprising:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of input selection devices for selecting one data from the plurality of input data in accordance with a control signal and supplying the same to different inputs of the first computing units,

at least one second computing unit each having a plurality of inputs and a plurality of outputs, supplied at the plurality of inputs with the output data of the plurality of first computing units, performing a plurality of operations based on the plurality of data

supplied in accordance with a control signal, and outputting the operation results from the plurality of outputs, and

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and at least one output data among the first and second computing units in accordance with a control signal.

39. An arithmetic device as set forth in claim 38, further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data in the plurality of input data and supplying the operation results to one input of the input selection device.

40. An arithmetic device as set forth in claim 38, wherein the plurality of output selection devices include

a plurality of first output selection devices each selecting and outputting one data from a plurality of input data and the output data of the first computing unit in accordance with a control signal and

a plurality of second output selection devices each selecting and outputting one data from the plurality of input data, the output data of the first computing unit, and the output data of the second computing unit in accordance with a control signal.

41. An arithmetic device as set forth in claim 38,

further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data in the plurality of input data and supplying the operation results to the output selection device.

42. An arithmetic device as set forth in claim 40, further comprising at least one monadic arithmetic means for performing monadic operation on predetermined data in the plurality of input data and supplying the operation results to the first output selection device.

43. An arithmetic device reconfigurable by outside control, comprising:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of first input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying the same to different inputs of the first computing units,

at least one second computing unit each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on a plurality of data supplied to the plurality of inputs in accordance

with a control signal, and outputting the operation results from the plurality of outputs, and

a plurality of second input selection devices each selecting one data from the plurality of input data and the output data of the second computing units in accordance with a control signal and supplying it to different inputs of the second computing unit.

44. An arithmetic device reconfigurable by outside control, comprising:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of first input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the first computing units,

at least one second computing unit having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on a plurality of data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of second input selection devices for selecting one data from the plurality of input data and the output data of the second computing unit in accordance with a control signal and supplying it to different inputs of the second computing unit, and

a plurality of output selection devices each selecting and outputting one data from a plurality of input data and at least one output data of the second computing unit in accordance with a control signal.

45. An arithmetic device reconfigurable by outside control, comprising:

a plurality of computing units, arranged in multiple stages, each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs and

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the plurality of computing units of the first stage,

the computing units arranged in stages other than the computing units of the first stage each being

supplied at the plurality of inputs with output data of the plurality of computing units of the previous stage, performing a plurality of operations based on the plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of outputs.

46. An arithmetic device reconfigurable by outside control, comprising:

a plurality of computing units, arranged in multiple stages, each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs and

a plurality of output selection devices each selecting and outputting one data from a plurality of input data and at least one output data of the computing units of the each stage in accordance with a control signal,

the computing units arranged in the stages other than the computing units of the first stage each being supplied at the plurality of inputs with output data of the plurality of computing units of the previous stage, performing a plurality of operations based on the

plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of outputs.

47. An arithmetic device as set forth in claim 46, wherein the plurality of output selection devices include

a plurality of first output selection devices each selecting and outputting one data from a plurality of input data and the output data of the computing unit of the first stage in accordance with a control signal and

a plurality of second output selection devices each selecting and outputting one data from the plurality of input data and the output data of the computing units of the different stages in accordance with a control signal.

48. An arithmetic device reconfigurable by outside control, comprising:

a plurality of computing units, arranged in multiple stages, each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on the data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of input selection devices each

selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the plurality of computing units of the first stage, and

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and at least one output data among the computing units of stages in accordance with a control signal,

the computing units arranged in the stages other than the computing units of the first stage each being supplied at the plurality of inputs with the output data of the plurality of computing units of the previous stage, performing a plurality of operations based on the plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of outputs.

49. An arithmetic device as set forth in claim 48, wherein the plurality of output selection devices include

a plurality of first output selection devices each selecting and outputting one data from a plurality of input data and the output data of the computing unit of the first stage in accordance with a control signal and

a plurality of second output selection devices

each selecting and outputting one data from the plurality of input data and the output data of the computing units of the different stages in accordance with a control signal.

50. A parallel arithmetic device, comprising:

a first arithmetic device reconfigurable by outside control having at least two selecting means each selecting desired data from a plurality of input data in accordance with a control signal and at least one arithmetic device including at least one arithmetic means for receiving output signals of the selecting means and performing operation in accordance with instructions of a control signal and

a second arithmetic device reconfigurable by outside control including at least one computing unit having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

the operation results of at least one of the first arithmetic device and second arithmetic device being supplied as input data of the other arithmetic device.

51. A parallel arithmetic device as set forth in

claim 50, wherein the first arithmetic device includes:

a first selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a second selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a third selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a first arithmetic means receiving as input the output signal of the first selecting means and the output signal of the second selecting means and performing operation in accordance with instructions of a control signal, and

a second arithmetic means receiving as input the output signal of the first selecting means and the output signals of the second selecting means and third selecting means and performing operation in accordance with instructions of a control signal.

52. A parallel arithmetic device as set forth in claim 51, wherein the first arithmetic device further comprises a fourth selecting means for selecting one of the output signal of the first arithmetic means and the output signal of the second arithmetic means in

accordance with a control signal.

53. A parallel arithmetic device as set forth in claim 50, wherein the first arithmetic device

includes a plurality of arithmetic devices and

connects the inputs and outputs of data of the plurality of arithmetic devices in cascade and supplies the operation result signal of an arithmetic device as one data of a plurality of data inputs of another device.

54. A parallel arithmetic device as set forth in claim 50, wherein the second arithmetic device comprises:

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the computing unit and

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and the output data of the computing unit in accordance with a control signal.

55. A parallel arithmetic device as set forth in claim 50, wherein the second arithmetic device includes:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from

the plurality of outputs,

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the find computing unit, and

at least one second computing unit having a plurality of inputs and a plurality of outputs, supplied at the plurality of inputs with output data of the plurality of first computing units, performing a plurality of operations based on the supplied plurality of data in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and at least one output data of the first and second computing units in accordance with a control signal.

56. A parallel arithmetic device as set forth in claim 50, wherein the second arithmetic device includes:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from

the plurality of outputs,

a plurality of first input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the first computing unit, and

at least one second computing unit having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on the plurality of data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of second input selection devices each selecting one data from the plurality of input data and the output data of the second computing units and supplying it to different inputs of the second computing units, and

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and at least one output data of the second computing units in accordance with a control signal.

57. A parallel arithmetic device as set forth in claim 50, wherein the second arithmetic device includes:

a plurality of computing units, arranged in multiple stages, each having a plurality of inputs and a plurality of outputs, performing a plurality of

operations based on the data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the plurality of computing units of the first stage, and

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and at least one output data among the computing units of stages in accordance with a control signal,

the computing units arranged in the stages other than the computing units of the first stage each being supplied at the plurality of inputs with the output data of the plurality of computing units of the previous stage, performing a plurality of operations based on the plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of outputs.

58. A parallel arithmetic device as set forth in claim 50, further comprising a means able to set any delay between the arithmetic devices.

59. A parallel arithmetic device, comprising:

a plurality of first arithmetic devices reconfigurable by outside control each having at least two selecting means each selecting desired data from a plurality of input data in accordance with a control signal and at least one arithmetic device including at least one arithmetic means for receiving output signals of the selecting means and performing operation in accordance with instructions of a control signal and

a plurality of second arithmetic devices reconfigurable by outside control each including at least one computing unit each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

the operation results of the plurality of first arithmetic devices being supplied to the corresponding second arithmetic devices and the operation results of the second arithmetic devices being supplied to the corresponding first arithmetic devices.

60. A parallel arithmetic device as set forth in claim 59, wherein the first arithmetic device includes:

a first selecting means for selecting desired

data from a plurality of input data in accordance with a control signal,

a second selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a third selecting means for selecting desired data from a plurality of input data in accordance with a control signal,

a first arithmetic means for receiving as input the output signal of the first selecting means and the output signal of the second selecting means and performing operation in accordance with instructions of a control signal, and

a second arithmetic means for receiving as input the output signal of the first selecting means and the output signals of the second selecting means and third selecting means and performing operation in accordance with instructions of a control signal.

61. A parallel arithmetic device as set forth in claim 60, wherein the first arithmetic device further comprises a fourth selecting means for selecting one of the first arithmetic means and the output signal of the second arithmetic means in accordance with a control signal.

62. A parallel arithmetic device as set forth in

claim 59, wherein the first arithmetic device includes a plurality of arithmetic devices, connects in cascade the inputs and outputs of data of the plurality of arithmetic devices, and supplies the operation result signal of each arithmetic device as one data of the plurality of data inputs of another device.

63. A parallel arithmetic device as set forth in claim 59, wherein the second arithmetic device comprises:

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the computing unit and

a plurality of output selection devices each selecting and outputting one data from the plurality of input data and the output data of the computing unit in accordance with a control signal.

64. A parallel arithmetic device as set forth in claim 59, wherein the second arithmetic device includes:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of input selection devices each

selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the first computing units,

at least one second computing unit each having a plurality of inputs and a plurality of outputs, supplied at the plurality of inputs with output data of the plurality of first computing units, performing a plurality of operations based on the plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of outputs, and

a plurality of output selection devices each selecting and outputting one data from a plurality of input data and at least one output data of the first and second computing units in accordance with a control signal.

65. A parallel arithmetic device as set forth in claim 59, wherein the second arithmetic device includes:

a plurality of first computing units each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of first input selection devices

each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the first computing units,

at least one second computing unit each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on the plurality of data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of outputs,

a plurality of second input selection devices each selecting one data from the plurality of input data and output data of the second computing unit in accordance with a control signal, and

a plurality of output selection devices each selecting and outputting one data from a plurality of input data and at least one output data of the second computing unit in accordance with a control signal.

66. A parallel arithmetic device as set forth in claim 59, wherein the second arithmetic device includes:

a plurality of computing units, arranged in multiple stages, each having a plurality of inputs and a plurality of outputs, performing a plurality of operations based on data supplied to the plurality of inputs in accordance with a control signal, and outputting the operation results from the plurality of

outputs,

a plurality of input selection devices each selecting one data from a plurality of input data in accordance with a control signal and supplying it to different inputs of the computing units of the first stage, and

a plurality of output selection devices each selecting and outputting one data from a plurality of input data and at least one output data of the computing units of the stages in accordance with a control signal,

the computing units arranged in stages other than the computing units of the first stage each being supplied at the plurality of inputs with output data of the plurality of computing units of the previous stage, performing a plurality of operations based on the plurality of data supplied in accordance with a control signal, and outputting the operation results from the plurality of outputs.

67. A parallel arithmetic device as set forth in claim 59, further comprising a means able to set any delay between arithmetic devices.

68. An arithmetic system, comprising:

a plurality of component data memories for storing different component data,

a data memory able to read and write at least

operation data in accordance with a designated address,

a selection device for selecting component data of the plurality of component data memories in accordance with a control signal,

an address generation device for, when receiving a startup signal, generating addresses of the data memory by a designated pattern, reading from the data memory and writing to the data memory, generating a control signal including selection information in accordance with the generated addresses, and outputting it to the selection device, and

an arithmetic device reconfigured based on component data selected by the selection device, performing predetermined operation on read data of the data memory, and outputting the operation results to the data memory as write data.

69. An arithmetic system as set forth in claim 68, wherein the address generation device performs a series of operations of reading data of the data memory for the amount of the generated addresses and rewriting the operation results in the data memory for the amount of generated addresses.

70. An arithmetic system as set forth in claim 68, wherein the address generation device comprises a control circuit for outputting a second control signal to the

selection device and able to dynamically change selected component data while generating addresses.

71. An arithmetic system as set forth in claim 69, wherein the address generation device comprises a control circuit for outputting a second control signal to the selection device and able to dynamically change selected component data while generating addresses

72. An arithmetic system, comprising:

a plurality of component data memories for storing different component data,

a data memory able to read and write at least operation data in accordance with a designated address,

a selection device for selecting component data of the plurality of component data memories in accordance with a control signal,

an address generation device for, when receiving a startup signal, generating an address of the data memory by a designated pattern, reading from the data memory and writing to the data memory, generating a control signal including selection information in accordance with the generated address, and outputting it to the selection device,

an arithmetic device reconfigured based on component data selected by the above selection device, performing predetermined operation on read data of the

data memory, and outputting the operation results to the data memory as write data, and

a control circuit for outputting a startup signal to the address generation device at a predetermined timing and designating an address pattern to be generated.

73. An arithmetic system as set forth in claim 72, wherein the control circuit is able to access the plurality of component data memories and data memory, writes the component data in the plurality of component data memories, outputs the second control signal to the selection device, decides whether to utilize the component data of the plurality of component data memories, writes the data of the data memory, then outputs the startup signal to the address generation device.

74. An arithmetic system as set forth in claim 72, wherein the address generation device performs a series of operations of reading data of the data memory for the amount of the generated addresses and rewriting the operation results in the data memory for the amount of generated addresses and notifies the completion of operation to the control circuit.

75. An arithmetic system as set forth in claim 73, wherein the address generation device performs a series

of operations of reading data of the data memory for the amount of the generated addresses and rewriting the operation results in the data memory for the amount of generated addresses and notifies the completion of operation to the control circuit.

76. An arithmetic system as set forth in claim 72, wherein while the address generation device is generating addresses, the control circuit outputs the second control signal to the selection device and able to dynamically change the selected component data.

77. An arithmetic system as set forth in claim 73, wherein while the address generation device is generating addresses, the control circuit outputs the second control signal to the selection device and able to dynamically change the selected component data.

78. An arithmetic system as set forth in claim 74, wherein while the address generation device is generating addresses, the control circuit outputs the second control signal to the selection device and able to dynamically change the selected component data.

79. An arithmetic system as set forth in claim 75, wherein while the address generation device is generating addresses, the control circuit outputs the second control signal to the selection device and able to dynamically change the selected component data.

80. An address generation device for generating an address of a memory, comprising:

a plurality of counters for setting a count value by a processed count value,

a plurality of arithmetic means provided corresponding to the counters, processing the count values of the counters corresponding to supplied step values in accordance with a control signal, and supplying the processed count values to the corresponding counters, and

an address arithmetic means for performing operation in accordance with a control signal on the count values of the plurality of counters and outputting the operation results as the address.

81. An address generation device as set forth in claim 80, further comprising a means for stopping the count operation of the counters in accordance with the operation results of the input parameters and the count values of the counters.

82. An address generation device as set forth in claim 80, further comprising a means for stopping the count operation of one counter in accordance with operation results between the count value of that one counter and the count value of another counter.

83. An address generation device as set forth in

claim 80, further comprising a means for resetting the counters in accordance with the operation results between the input parameters and the count value of the counter.

84. An address generation device as set forth in claim 81, further comprising a means for resetting the counters in accordance with the operation results between the input parameters and the count value of the counter.

85. An address generation device as set forth in claim 80, further comprising a means for resetting one counter in accordance with operation results between the count value of that one counter and the count value of another counter.

86. An address generation device as set forth in claim 82, further comprising a means for resetting one counter in accordance with operation results between the count value of that one counter and the count value of another counter.

87. An address generation device as set forth in claim 82, further comprising a means able to freely designate initial values of the plurality of counters.

88. An address generation device as set forth in claim 80, further comprising a means able to temporarily stop countup of all of the counters in accordance with a control signal.

89. An address generation device for generating an

address of a memory accessed by an arithmetic device, comprising:

a plurality of counters for setting a count value by a processed count value,

a plurality of arithmetic means provided corresponding to the counters, processing the count values of the counters corresponding to supplied step values in accordance with a control signal, and supplying the processed count values to the corresponding counters,

an address arithmetic means for performing operation in accordance with a control signal on the count values of the plurality of counters and outputting the operation results as the address, and

a control signal generating means for generating a control signal of the arithmetic device based on the count values of the plurality of counters.

90. An address generation device as set forth in claim 89, wherein:

the device comprises a means for stopping the count operations of the counters in accordance with the operation results between the input parameters and the count values of the counters, while

the control signal generating means generates a control signal based on the operation results of the means for stopping the count operations.

91. An address generation device as set forth in claim 89, wherein:

the device comprises a means for stopping the count operation of one counter in accordance with the operation results between the count value of that one counter and the count value of another counter, while

the control signal generating means generates a control signal based on operation results of the means for stopping the count operation.

92. An address generation device as set forth in claim 89, further comprising a means for resetting a counter in accordance with operation result between an input parameter and count value of the counter.

93. An address generation device as set forth in claim 90, further comprising a means for resetting a counter in accordance with operation results between an input parameter and count value of the counter.

94. An address generation device as set forth in claim 89, further comprising a means for resetting one counter in accordance with operation results between a count value of that one counter and a count value of another counter.

95. An address generation device as set forth in claim 91, further comprising a means for resetting one counter in accordance with operation results between a

count value of that one counter and a count value of another counter.

96. An address generation device as set forth in claim 89, further comprising a means able to designate any initial value of the plurality of counters.

97. An address generation device as set forth in claim 89, further comprising a means able to temporarily stop countup of all counters in accordance with a control signal.

98. An interleave device, comprising:

at least one delay means able to insert any delay cycles into a plurality of input data and

a plurality of selecting means for selecting as output data any of the input data and the output of the delay means in accordance with a control signal.

99. An interleave device, comprising:

a first delay means able to insert delay of predetermined cycles into first input data,

a second delay means able to insert delay of predetermined cycles into second input data,

a first selecting means for selecting as the first output data one of the first input data, second input data, output data of the first delay means, and output data of the second delay means, and

a second selecting means for selecting as the

second output data one of the first input data, second input data, output data of the first delay means, and output data of the second delay means.

100. An interleave device, comprising:

a first delay means for causing the first read data input from a first memory bank to be delayed by predetermined cycles,

a second delay means for causing the second read input from a second memory bank to be delayed by predetermined cycles,

a first selecting means for selecting as first read output the value of one of the first read data input, second read data input, output data of the first delay means, and output data of the second delay means in accordance with a control signal, and

a second selecting means for selecting as second read data output the value of one of the first read data input, the second read data input, the output data of the first delay means, and the output data of the second delay means in accordance with a control signal.

101. An interleave device for a plurality of read data input from a plurality n ($n \geq 3$) of memory banks, comprising:

a plurality of delay means provided corresponding to the read data inputs and able to insert

delay of any cycles and

a plurality of selecting means for selecting as read data output any of the a plurality of read data inputs and output data of the delay means in accordance with a control signal.

102. An interleave device as set forth in claim 101, wherein the delay means generates a delay of m cycles ($1 \leq m \leq n$) with respect to the read data input.

103. An interleave device, comprising:

a first delay means for delaying a first write data input from a first series by predetermined cycles,

a second delay means for delaying a second write data input from a second series by predetermined cycles,

a first selecting means for selecting the value of any of the first write data input, second write data input, output data of the first delay means, and output data of the second delay means, as write data output for the first memory bank in accordance with a control signal, and

a second selecting means for selecting the value of any of the first write data input, second write data input, output data of the first delay means, and output data of the second delay means as write data for the second memory bank in accordance with a control

signal.

104. An interleave device for a plurality of write data from a plurality n ($n \geq 3$) of series, comprising:

a plurality of delay means able to insert delay of any cycles in the write data inputs and

a plurality of selecting means for selecting any of the plurality of write data inputs and output data of the delay means as write data output for the corresponding memory banks in accordance with a control signal.

105. An interleave device as set forth in claim 104, wherein the first delay means gives delay of m cycles ($1 \leq m \leq n$) to the read data input.

106. An arithmetic system, comprising:

an arithmetic execution unit reconfigured based on supplied component data and performing predetermined operation on predetermined data,

a component data storage unit in which a plurality of storage means able to store component data connected in a ring and able to shift the stored data, supplies the component data stored in one storage means to the arithmetic execution unit, and component data is written in another strage means, and

a control means for writing component data in predetermined storage means of the component data storage

unit.

107. An arithmetic system as set forth in claim 106, wherein the control means shifts component data stored in the storage means of the component data storage unit to the storage means of the next stage in accordance with a shift signal and changes the component data to be supplied to the arithmetic execution unit.

108. An arithmetic system, comprising:

an arithmetic execution unit reconfigured based on supplied component data and performing predetermined operation on predetermined data,

a component data storage unit including a plurality of registers including a first register able to store component data connected in a ring and to be able to shift the stored data upon receipt of a shift signal and supplying the stored component data to the arithmetic execution unit and a second register able to rewrite component data upon receipt of a write signal and a selecting means for supplying component data to be written to the second register at the time of a write operation receiving a write signal and supplying component data stored in a register of the previous stage to the second register at the time of being written, and

a control means for transmitting a write signal and component data to be written to the component data

storage unit and rewriting the component data of the second register.

109. An arithmetic system as set forth in claim 108, wherein the control means shifts the component data stored in each register of the component data storage unit to a register of the next stage by a shift signal and changes the component data to be supplied to the arithmetic execution unit.